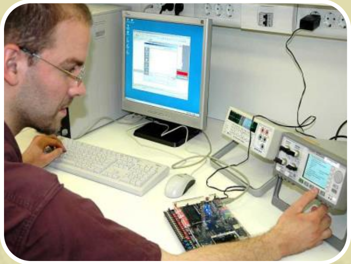
MŰEGYETEM 1782

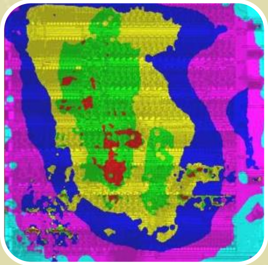
Budapest University of Technology and Economics

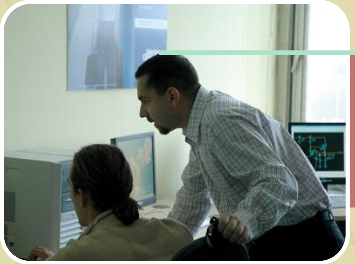
A fonzisztor - egy termikus-elektronikus aktív eszköz.

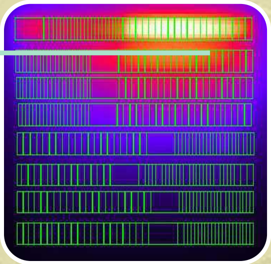
Thermal (nano?) electronics

Department of Electron Devices









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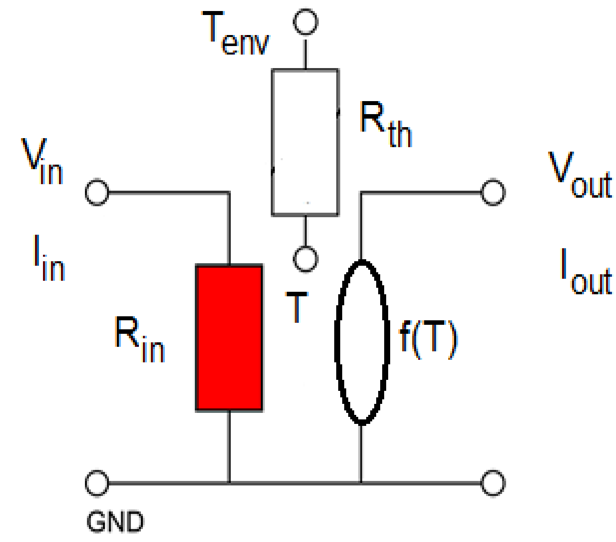
Outline

- electro-thermal integrated circuit: basic concept
- the MIT effect
- MIT resistor as memristor
- new thermal-electric device (phonsistor) and the
- (CMOS compatible) thermal-electric logic circuit (TELC)
- nanosized CMOS versus TELC
- analogy between neurons and TELC
- some measured results (thermal OR and AND gate)
- S/W analysis

$$T - T_{env} = \frac{V_{in}^2}{R_{in}} R_{th}$$

$$T - T_{env} = I_{in}^2 R_{in} R_{th}$$



$$\beta = \frac{\partial I_{out}}{\partial I_{in}} = \frac{\partial I_{out}}{\partial T}\frac{\partial T}{\partial I_{in}} = 2 I_{in} R_{in} R_{th} \frac{\partial I_{out}}{\partial T}$$

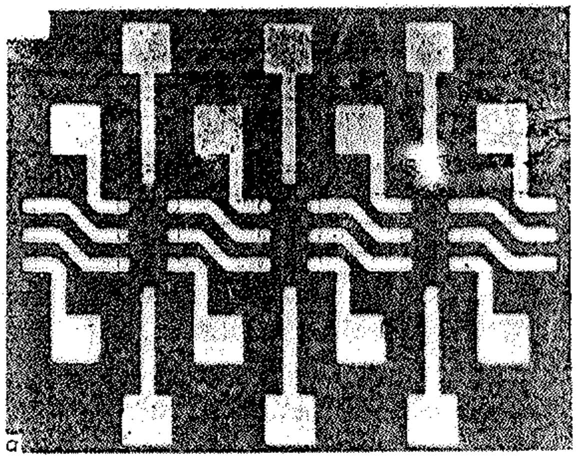
$$g_m = \frac{\partial I_{out}}{\partial V_{in}} = \frac{\partial I_{out}}{\partial T}\frac{\partial T}{\partial V_{in}} = 2 V_{in} \frac{R_{th}}{R_{in}} \frac{\partial I_{out}}{\partial T}$$

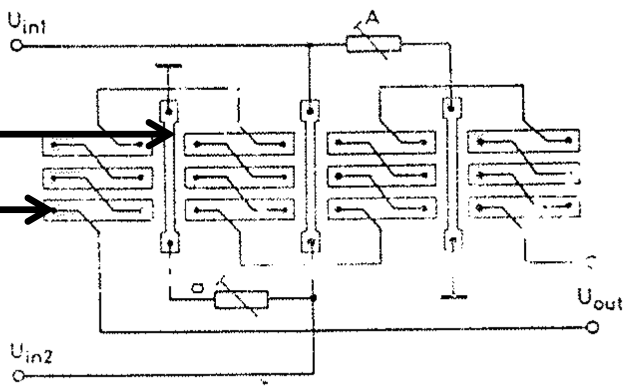
$$A = \frac{\partial V_{out}}{\partial V_{in}} = \frac{\partial V_{out}}{\partial T}\frac{\partial T}{\partial V_{in}} = 2 V_{in} \frac{R_{th}}{R_{in}} \frac{\partial V_{out}}{\partial T}$$

R_{th}

$\frac{\partial}{\partial T}$

Electro-thermal integrated circuit: the thermal-function 4-quadrant multiplier





a

b

Fig. 2 *Experimental thermal multiplier*

a Photomicrograph of the circuit. The overall dimensions are 710 × 560 μm
b Connection for the multiplier operation

diffused resistance heaters

arrays of Si-Al contacts

$$V_{out} = V_{in}^2 NS \frac{R_{th}}{R_{in}}$$

$$A = \frac{\partial V_{out}}{\partial V_{in}} = 2V_{in} \frac{R_{th}}{R_{in}} NS$$

Performance data: A single q.t.c. block (detail according to Fig. 1) gives a sensitivity of about 72 μV/mW. The input resistance of the multiplier connected as shown in Fig. 2*b* is 1·1 kΩ, whereas its output resistance is 11 kΩ. The relation between the input and output d.c. voltages is

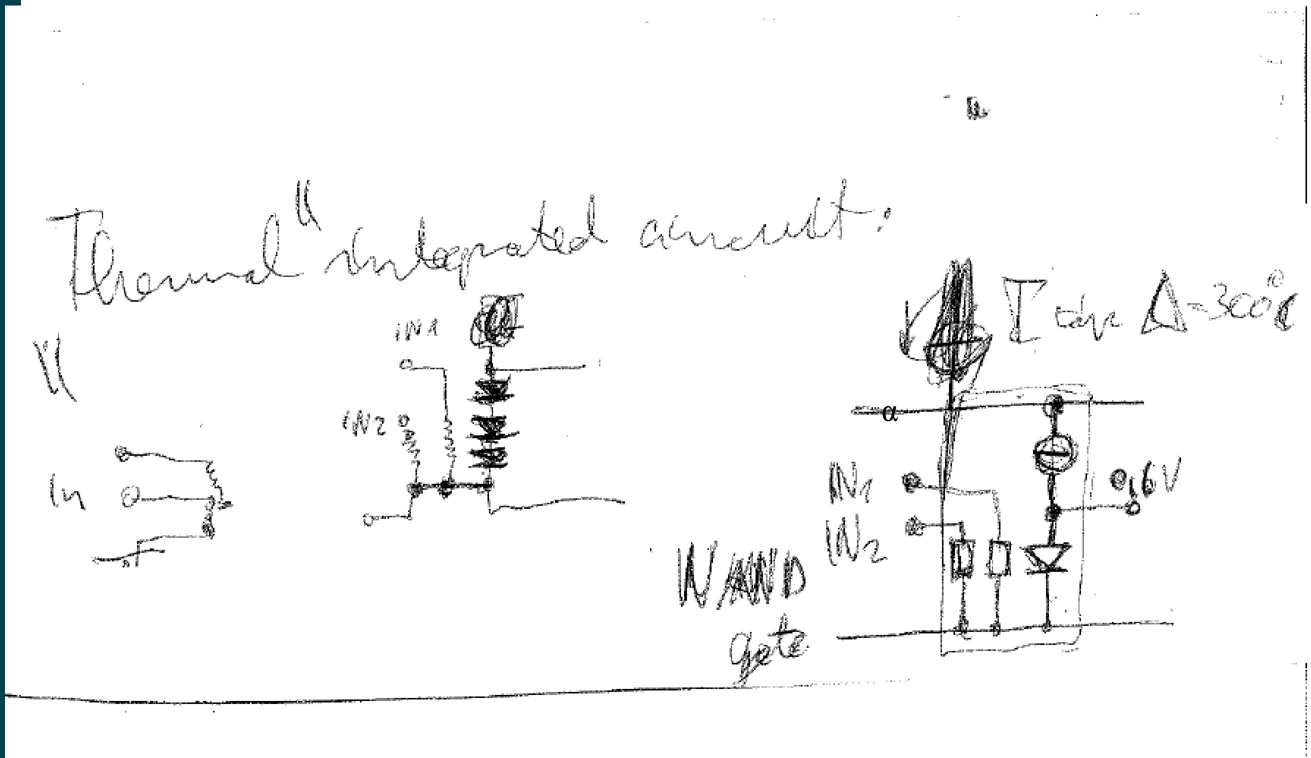
$$U_{OUT} = 6 \times 10^{-5} \times U_{IN1} U_{IN2} \qquad (4)$$

in volts. Fig. 3 demonstrates the good linearity of the experimental multiplier.

A distinct feature of the circuit is that the cutoff frequency for input signals is greater by orders of magnitude than that

Author: V. Székely Technical University of Budapest

Electro-thermal integrated circuit: basic concept (TCL: thermally coupled logic)

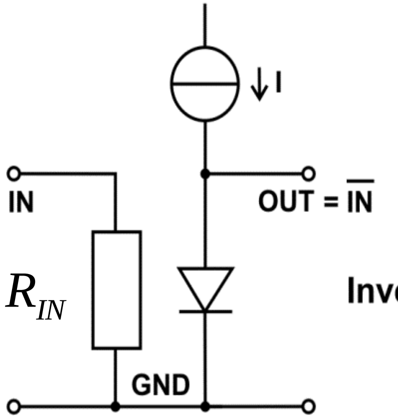


$$V_{out} = V_F - \alpha \frac{V_{in}^2}{R_{in}} R_{th}$$

$$A = \frac{\partial V_{out}}{\partial V_{in}} = 2V_{in} \frac{R_{th}}{R_{in}} \alpha$$

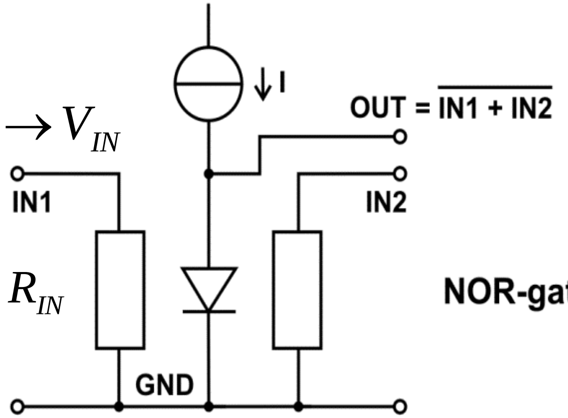
Electro-thermal integrated circuit: basic concept (TCL: thermally coupled logic)

$$\alpha\Delta T = \alpha P R_{th} = \alpha I^2 \cdot R_{IN} R_{th} \geq V_F$$ → to switch on the gate



Inverter

$V_{OUT} \rightarrow V_{IN}$



NOR-gate

Problems: low power gain, signal regeneration, fan-out.

Something different is needed, instead of simple pn junctions!

$$V_{OUT} \rightarrow V_{IN} = V_F - \alpha \frac{V_{IN}^2}{R_{IN}} R_{th}$$ → to switch on the next gate

previous next

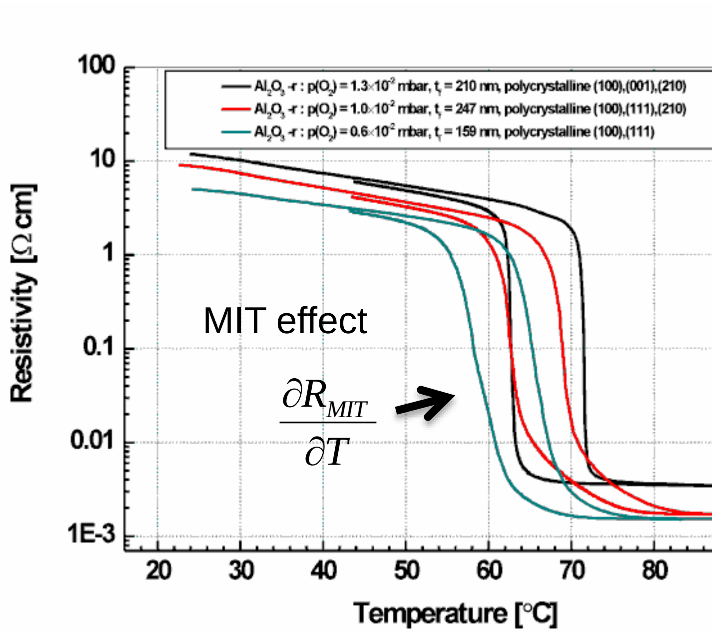
The forward voltage of silicon diodes (p-n junctions) decrease about α=2 mV/K at a constant forward current The early idea for thermal-electronic logic circuit (TELC) operates with p-n junctions and control resistors. Either of input resistors is heated up, the output voltages decrease (NOR logic function).

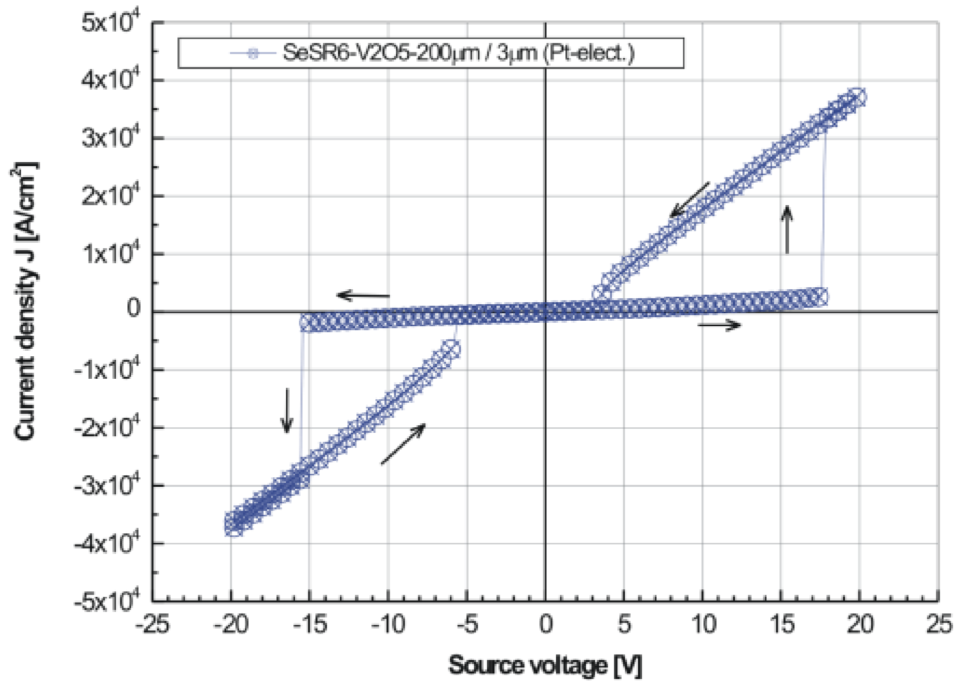
$$\alpha\Delta T = \alpha P R_{th} = \alpha I V_F R_{th} << V_F$$ → avoid to thermal switch on the pn junction itself

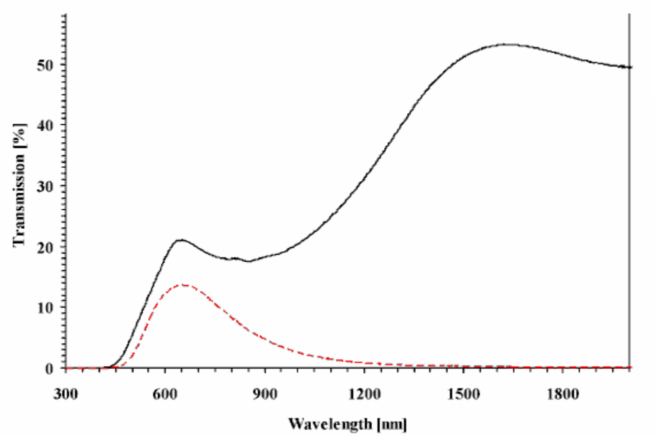
$$I \cdot R_{IN} < V_F$$ → avoid to electrical switch on the pn junction itself

Previous next previous

Metal-Insulator-Transition (MIT) VO_2 thin films:

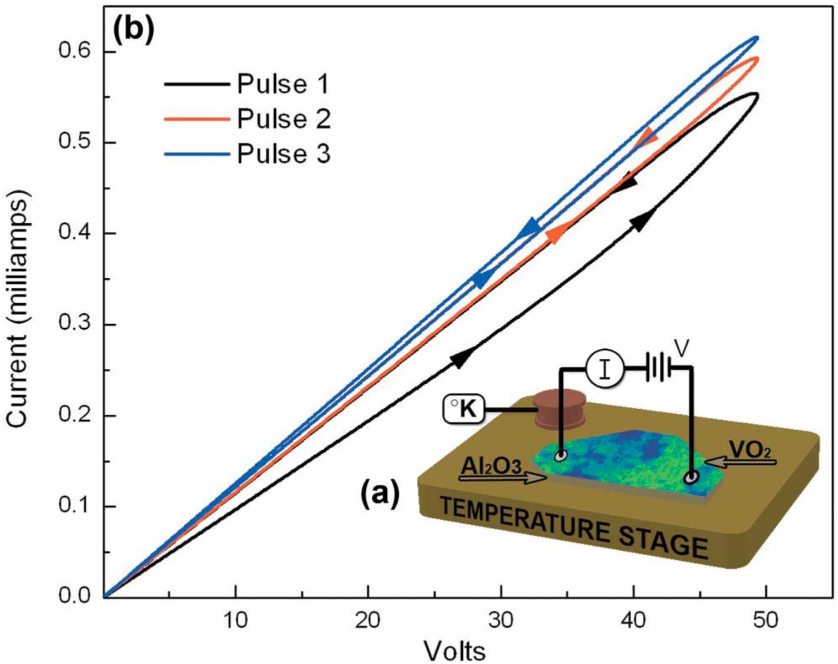


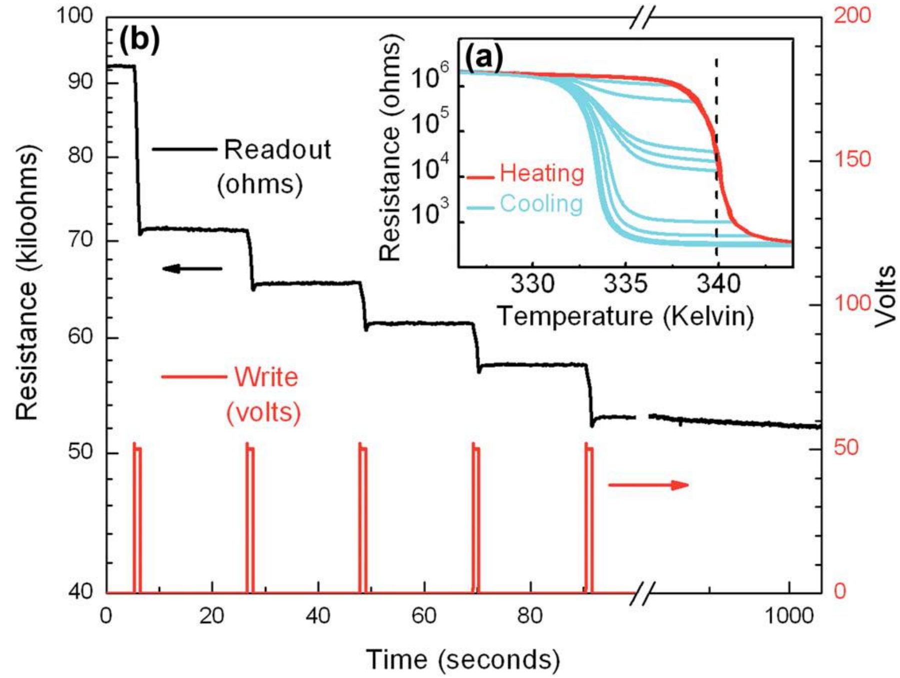


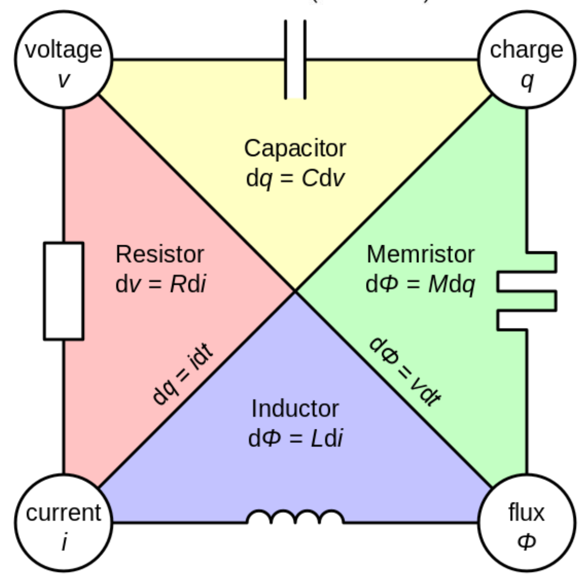


Optical and electrical switching characteristics of MIT effect induced by Joule-heating method. Very high optical density films with T(λ)≈ 0 @ 1550 μm in metal state(red line).

MIT memristive effect



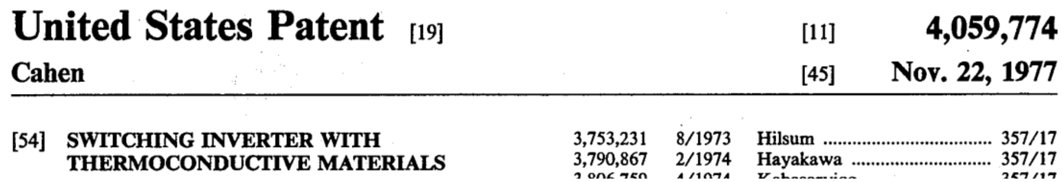




resistor: no memory, ohmic
capacitor: charge memory
inductor: current memory
memristor: charge memory, ohmic

Applications

- (New) functional device by thermal coupling (phonon coupler, phonsistor).

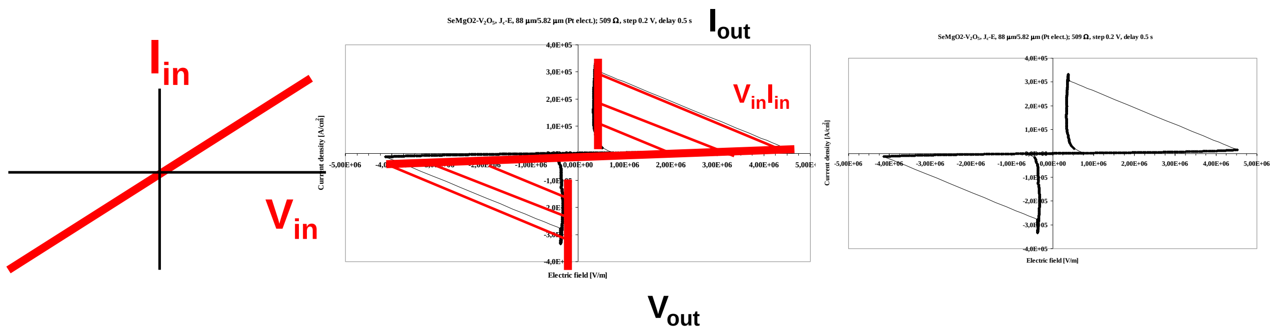


United States Patent [19] [11] 4,059,774

Cahen [45] Nov. 22, 1977

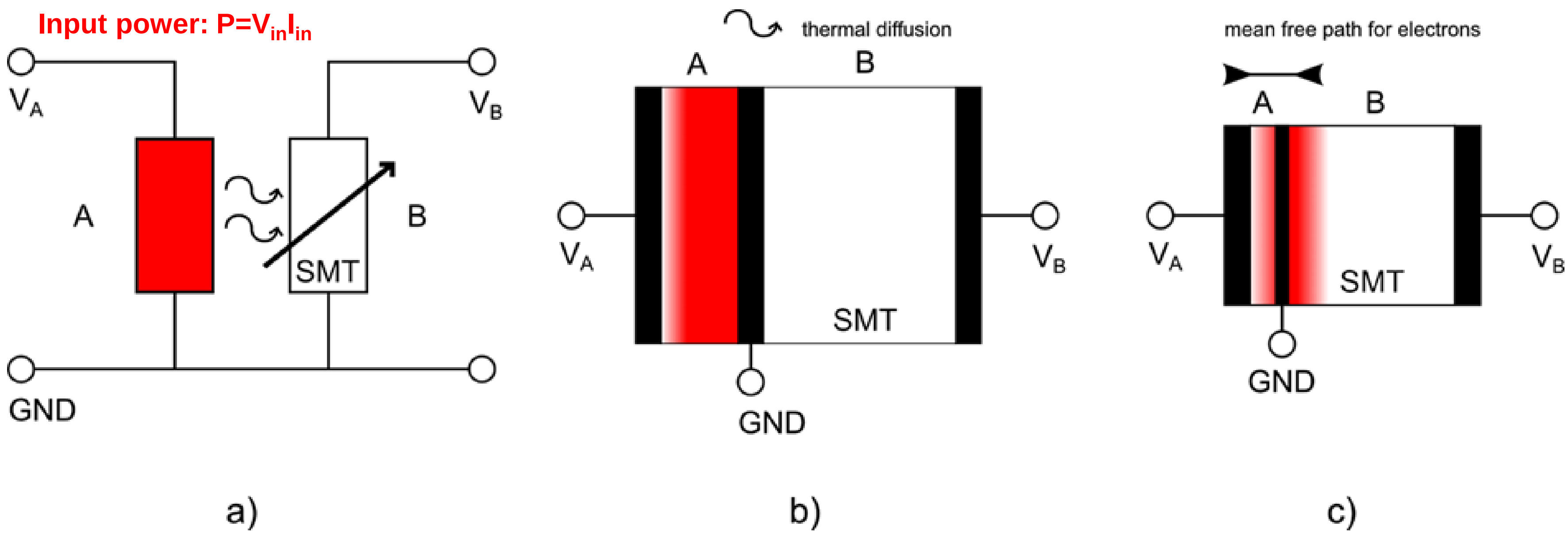
[54] SWITCHING INVERTER WITH THERMOCONDUCTIVE MATERIALS

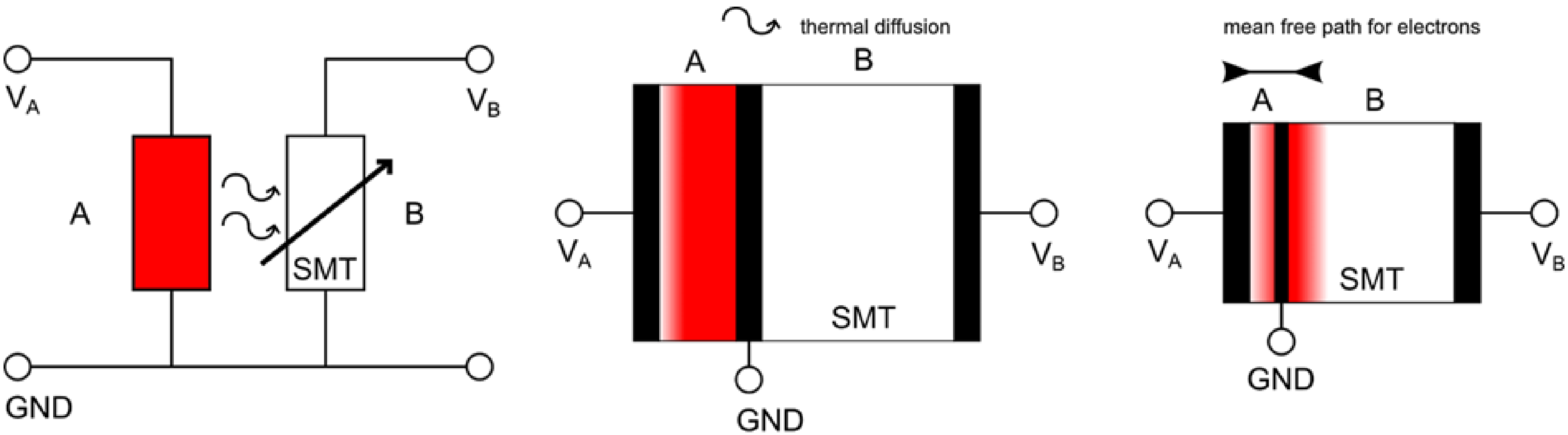
3,753,231	8/1973	Hilsum	357/17
3,790,867	2/1974	Hayakawa	357/17



Properties of the phonsistor:
- active device
- ohmic input and
- thyristor-like output characteristics
- it saves the output state

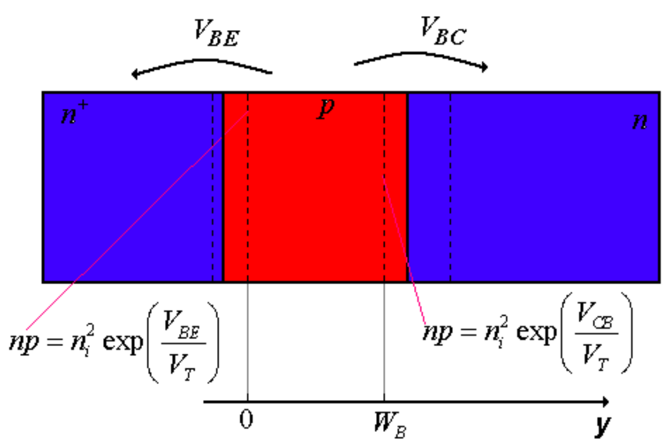
Ballistic transport, thermalisation in the SMT:



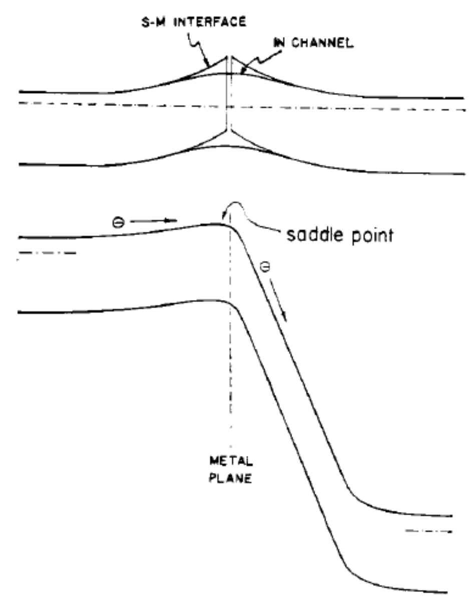


a) b) c)

minority carrier diffusion

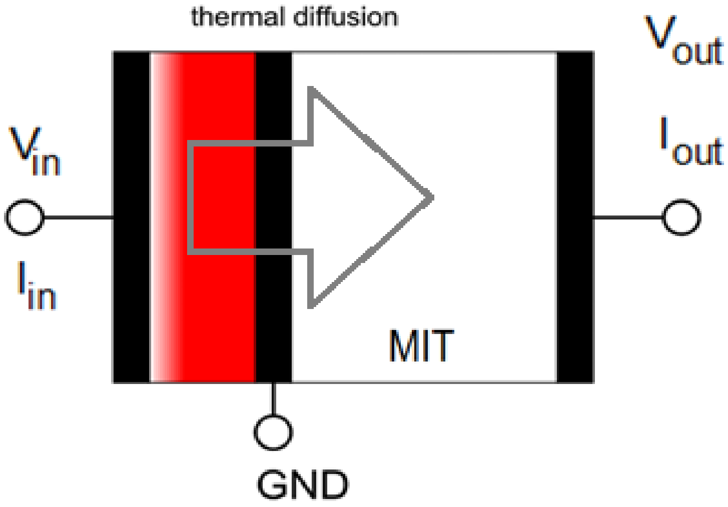


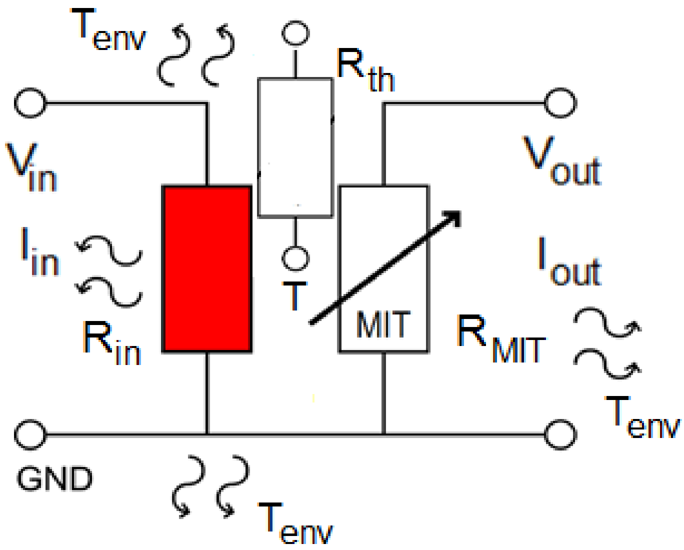
ballistic transport of electrons through the metal base

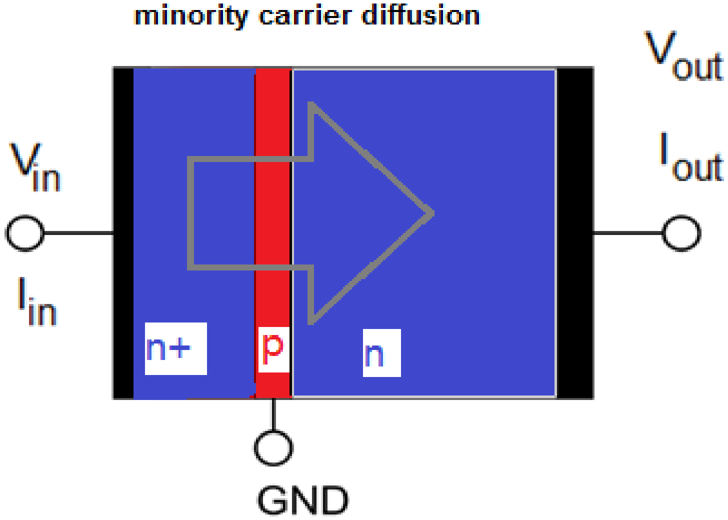


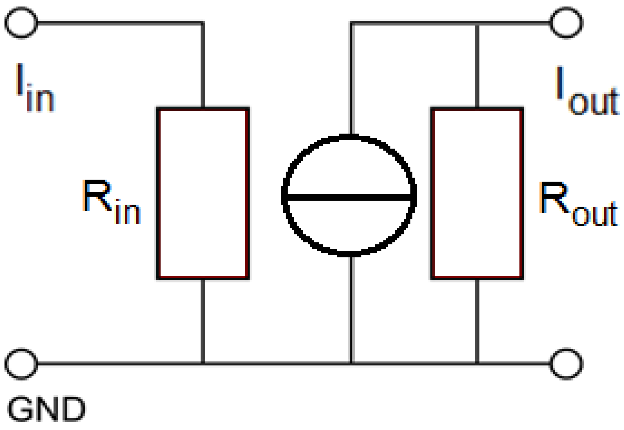
Bipolar transistor and metal base transistor analogy

Phonsistor – bipolar transistor









Using V as power supply:

$$I_{out} = \frac{V}{R_{MIT}(T)} = \frac{V}{R_{MIT}\left(T_{env} + I_{in}^2 R_{in} R_{th}\right)} = \frac{V}{R_{MIT}\left(T_{env} + \dfrac{V_{in}^2}{R_{in}} R_{th}\right)}$$

$$\beta = \frac{\partial I_{out}}{\partial I_{in}} = \frac{\partial I_{out}}{\partial T}\frac{\partial T}{\partial I_{in}} = 2 I_{in} R_{in} R_{th} \frac{V^2}{R_{MIT}} \frac{\partial R_{MIT}}{\partial T}$$

$$g_m = \frac{\partial I_{out}}{\partial V_{in}} = \frac{\partial I_{out}}{\partial T}\frac{\partial T}{\partial V_{in}} = 2 V_{in} \frac{R_{th}}{R_{in}} \frac{V^2}{R_{MIT}} \frac{\partial R_{MIT}}{\partial T}$$

$(V_{in})^2/R_{in}$) is much higher than the power dissipated on the MIT resistor ($I^2 R_{MIT}$)

Using I as power supply:

$$V_{out} = IR_{MIT}(T) = IR_{MIT}\left(T_{env} + \frac{V_{in}^2}{R_{in}} R_{th}\right)$$

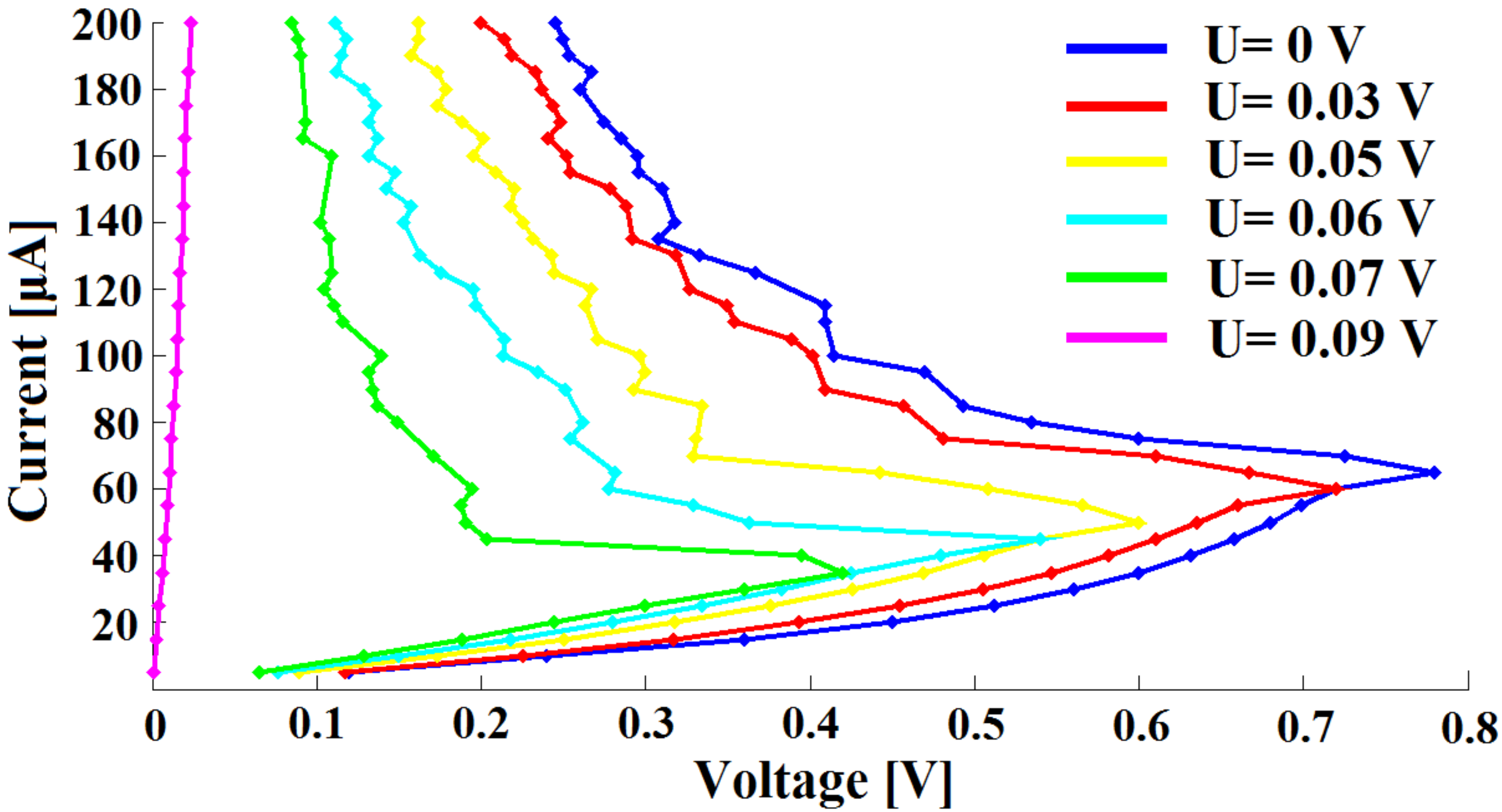
$$A = \frac{\partial V_{out}}{\partial V_{in}} = I\,\frac{\partial R_{MIT}(T)}{\partial T} \cdot \frac{\partial T}{\partial V_{in}} = 2V_{in} I \cdot \frac{\partial R_{MIT}}{\partial T} \cdot \frac{R_{th}}{R_{in}}$$

$(V_{in})^2/R_{in}$) is much higher than the power dissipated on the MIT resistor (I^2R_{MIT})

High signal condition at the output:

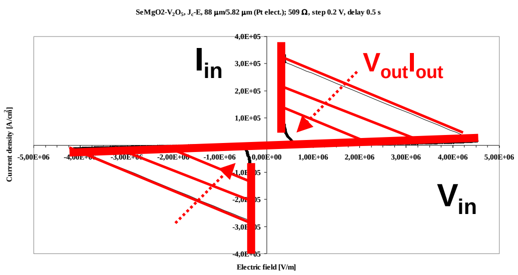
$(V_{in})^2/R_{in}) \sim (I^2 R_{MIT})$

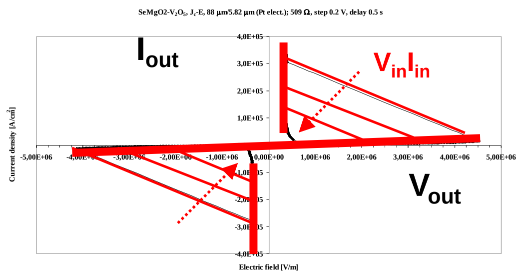
$$V_{out} = IR_{MIT}\left(T_{env} + \frac{V_{in}^2}{R_{in}}R_{th} + I^2 R_{th} R_{MIT}\left(T_{env} + \frac{V_{in}^2}{R_{in}}R_{th} + I^2 R_{th} R_{MIT}\left(T_{env} + \frac{V_{in}^2}{R_{in}}R_{th} + \ldots\right)\right)\right)$$



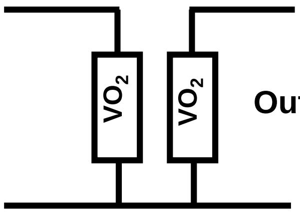
Applications

- New functional device by mutual thermal coupling (reciproque phonsistor).





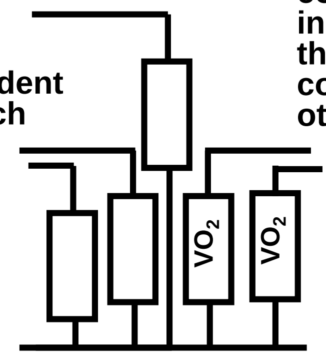
Input (?)



Output (?)

- New functional logic cell by mixed thermal coupling

Input(s), independent from each other

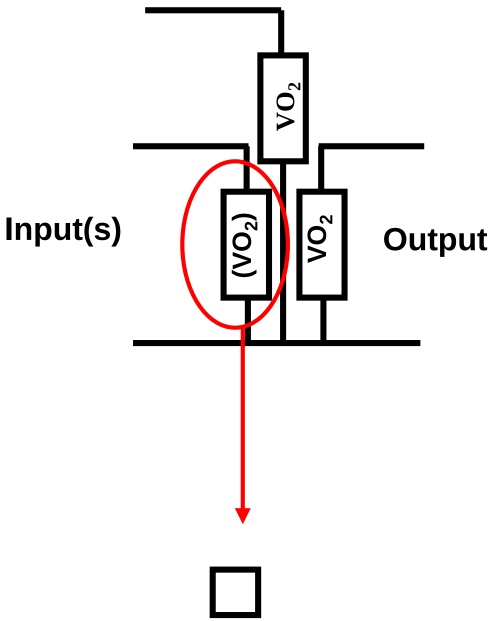


Output(s), controlled by input(s), but they can control each other too

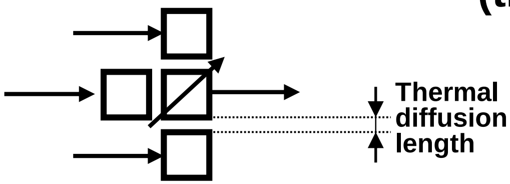
Properties:
- active device (thyristor-like characteristics),
- it saves both input and output states
- symmetric (symmetry depends on size of the resistors)
- and “reciproque” (“input” can be switched on from the “output”, too) !
- the output conditions can be seen from the input side, too !

Thermally coupled logic (TCL)→ next slides!

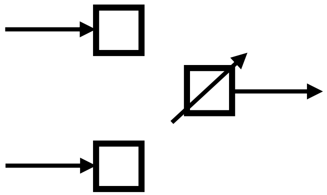
Electro-thermal integrated circuit: basic concept (TCL: thermally coupled logic)



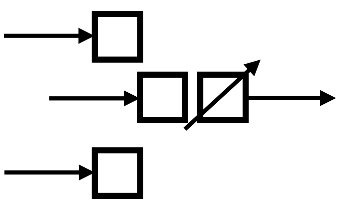
- OR gate: (three input)



- AND gate:



- Complex (AND OR) gate:



Patent (phonsistor, thermal-electric integrated circuit) submitted to the Hungarian Patent Office by the **Budapest University of Technology and Economics**

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Iktatás

Iktatószám	Iktatás dátum	Iktatta
1214229	2012.04.27.	Káldi M.

P.fdat: Szabadalom / Bejelentés*

Ügyszám: P1200249
Ügyiratszám: P1200249 / 1
Ügyintéző:
Benyújtó: BUDAPESTI MŰSZAKI ÉS GAZD
Képviselő: Gödölle,Kékes,Mészáros & Szabó Szabadalm
Tárgy: LOGIKAI ELRENDEZÉS

Benyújtott iratok:

Bejelentési kérelem	(db)	1
Leírás	(db)	3
Igénypont	(db)	3
Rajz	(db)	21
Kiv[illegible]t	(db)	3
Melléklet	(db)	1

SZELLEMI TULAJDON NEMZETI HIVATALA * XVI *

Thermal diffusivity: $$\alpha = \frac{k}{\rho c_p}$$

In heat transfer analysis, **thermal diffusivity** (symbol: α) is the ratio of thermal conductivity to volumetric heat capacity.

where:

- k : thermal conductivity (SI units: W/(m K))
- ρc_p : volumetric heat capacity (SI units: J/(m^3K))
- ρ : density (SI units: kg/(m^3))
- c_p : specific heat capacity (SI units: J/(kg K))

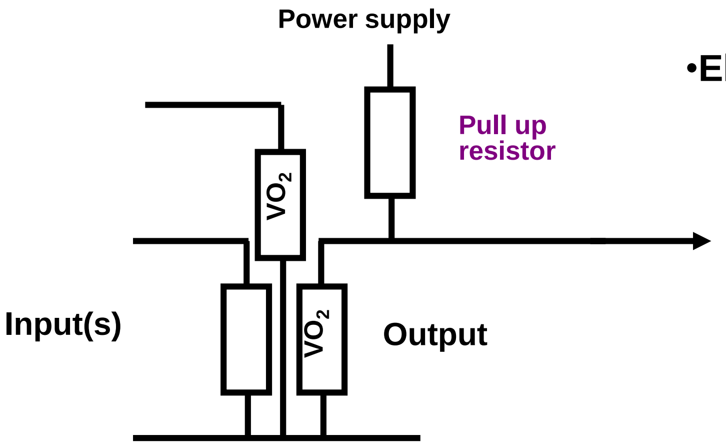
Thermal diffusion length (characteristic lenght at given time scale):

$$L_{th} = \sqrt{\alpha t}$$

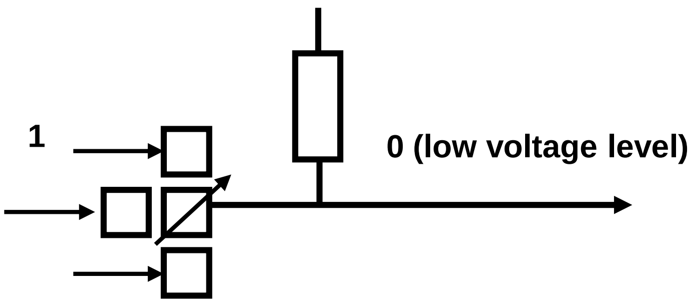
$\alpha \sim 10^{-6}$ m^2/s (SiO_2), time is 10^{-10} sec, than $L_{th}=10^{-8}$ m (10nm)

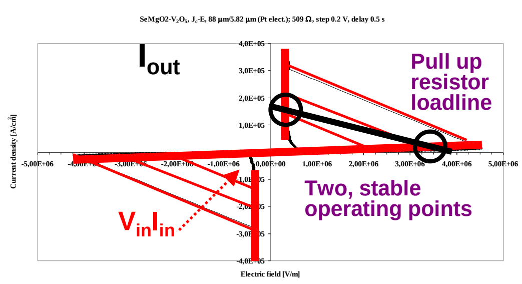
$\alpha \sim 6 x 10^{-5}$ m^2/s (Si), time is 10^{-10} sec, than $L_{th}=7x10^{-8}$ m (70nm)

Electro-thermal integrated circuit: a bit more…

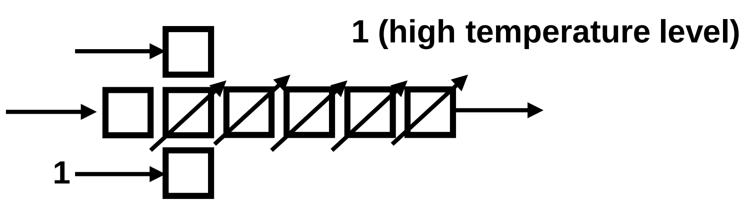


- Electrical coupling: NOR



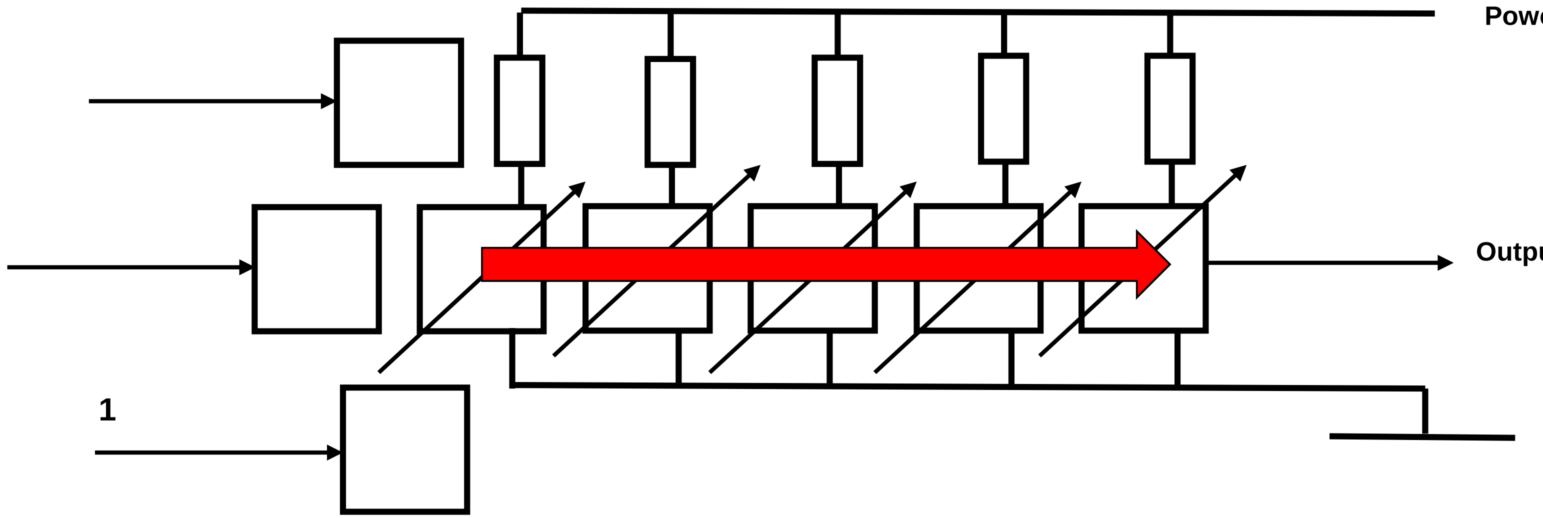


- Thermal coupling: OR



Practical realisation: vertical (three dimensional thermal IC, possibly stacked, see more later)

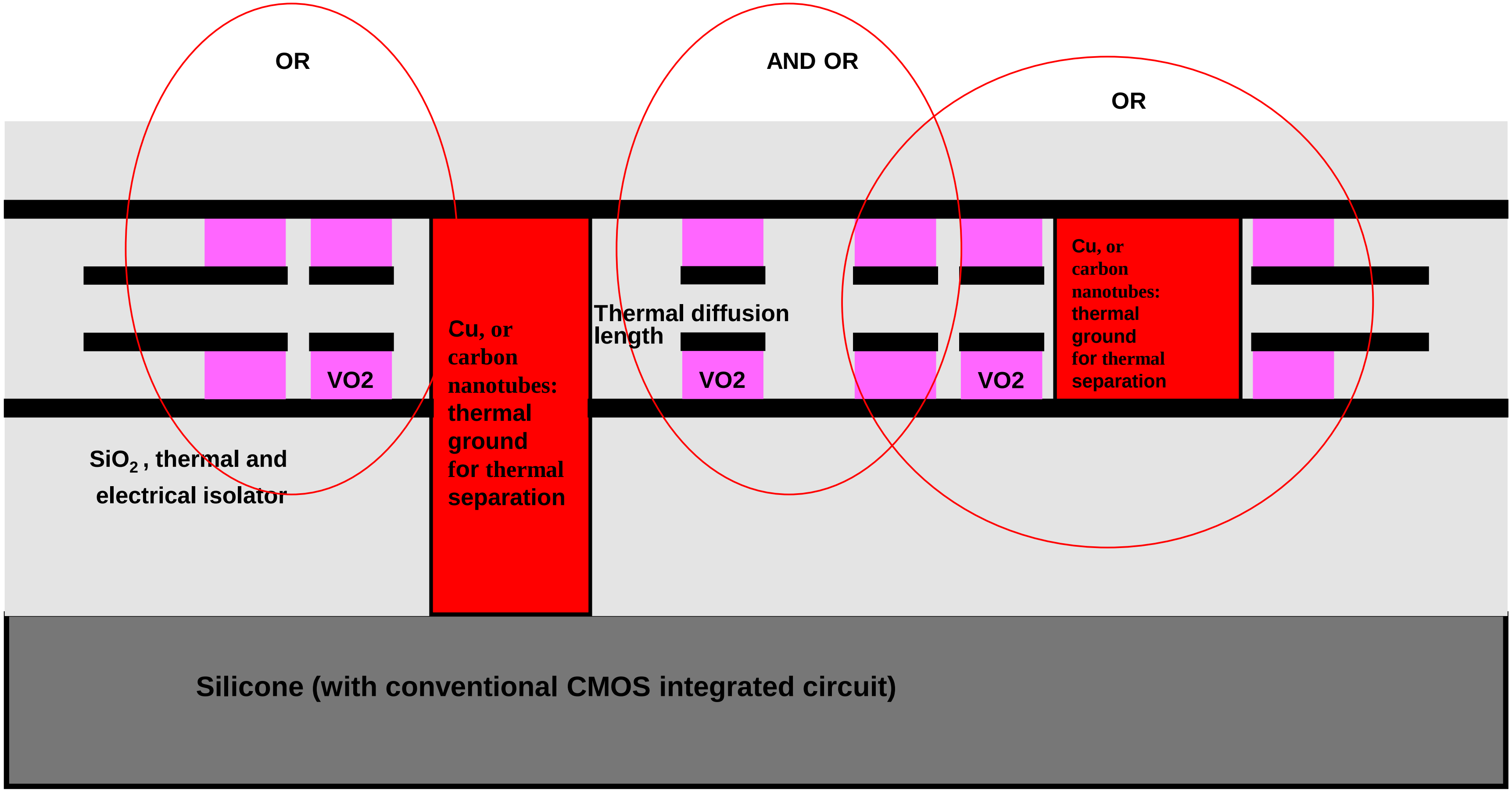
Electro-thermal integrated circuit: thermal transmission line with three OR/NOR input



propagation of the thermal „1” state, signal regeneration

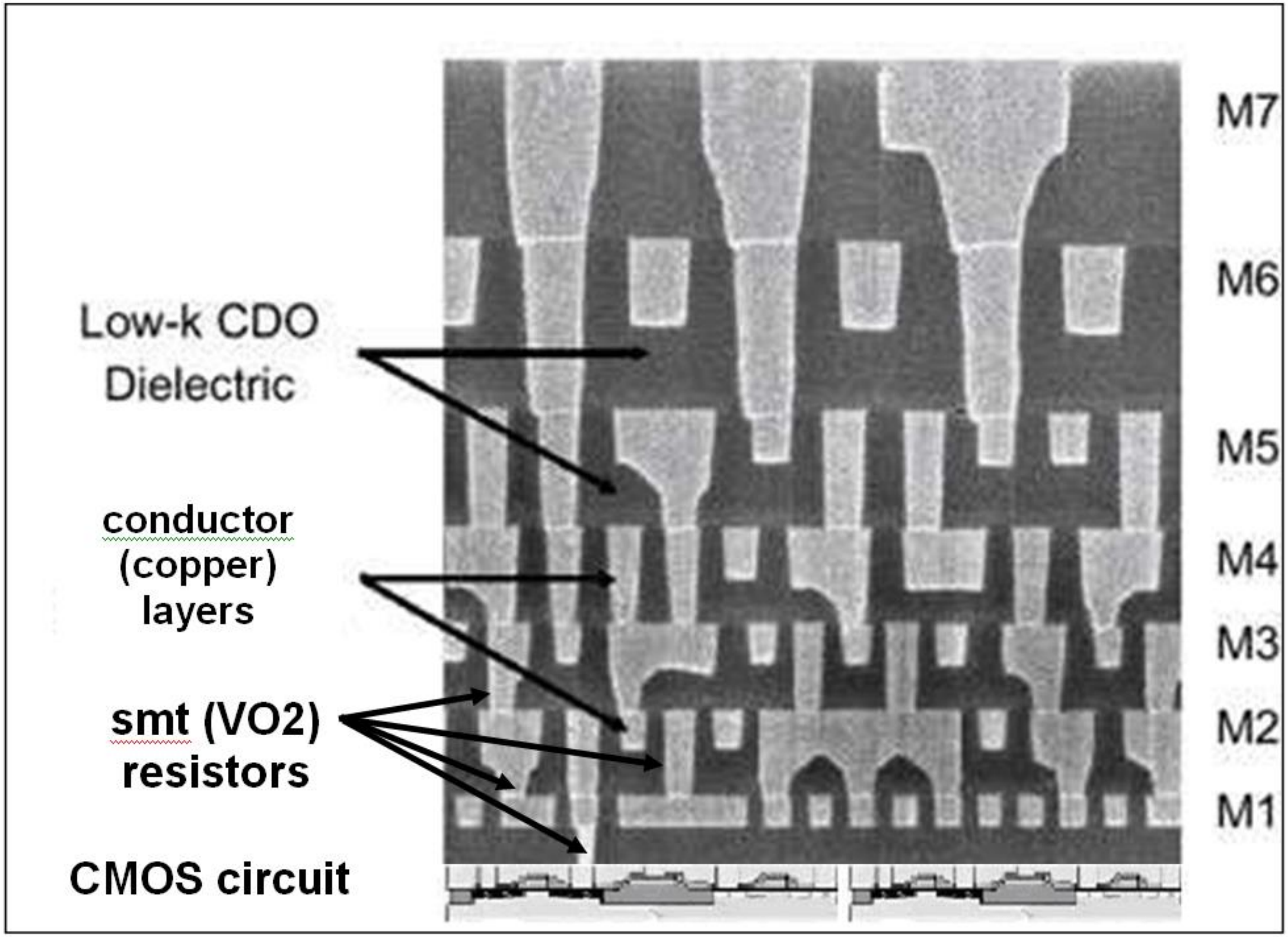
Some ideas for practical realisations:

Vertical (three dimensional thermal IC), cross section:



Some ideas for practical realisations: CMOS compatibility

Vertical (three dimensional thermal and CMOS IC), cross section:



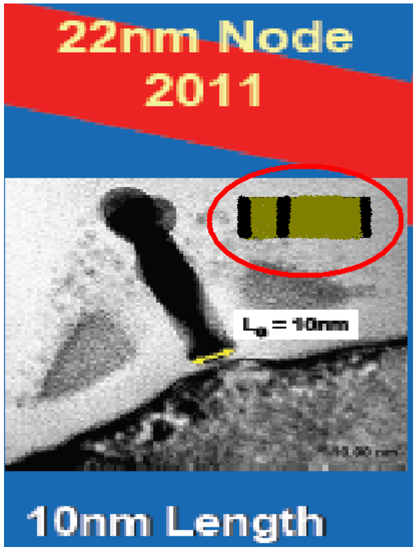
Some ideas for practical realisations: real size and scalability

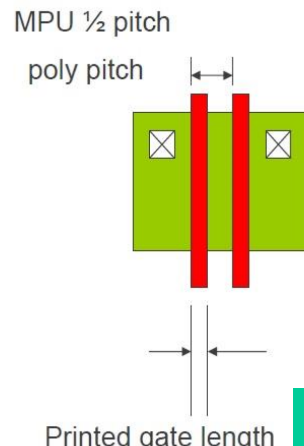
C. Piguet

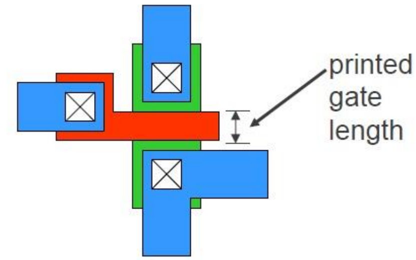
In 2020

ITRS (roadmap)

- 90 nm — 2002
- 65 nm — 2006
- 45 nm — 2008
- 32 nm — 2010
- 22 nm — 2011
- 16 nm — 2013
- 11 nm — approx. 2015







In 2020:
- ½ half pitch: **14 nanometers**
- printed gate length: **9 nanometers**
- physical gate length: **6 nanometers**

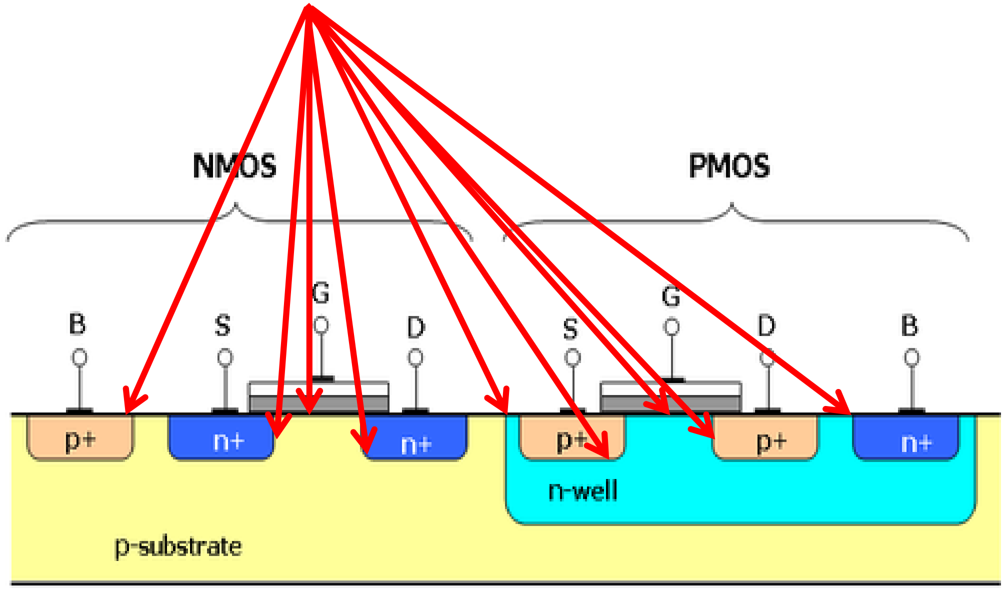
Phonsistor size:

	Geometry, volume	Power supply voltage	Clock frequency	Number of components
Recent CMOS gate properties:	(22+22)x50x50 nm, 110000 nm^3	0.8-0.7 V	4 GHz	**2 (“driver-loader”)**
Theoretical limits (over-estimated) for CMOS:	(11+11)x30x30 nm (3D) 19800 nm^3	0.5 V	6 + (?) GHz	**2 (“driver-loader”)**
Estimated limits for TELC:	**10x10x30 nm (3D) 3000 nm^3**	**0.4- 0.2 V**	**10 Ghz**	**1 (functional device)**

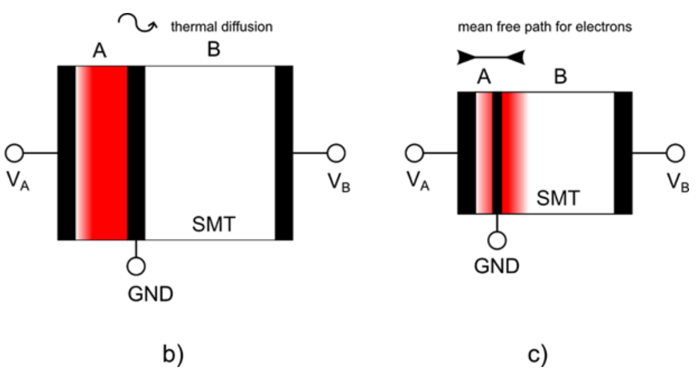
Problems with CMOS: typical surface device

Phonsistor: simple bulk device

device limits (6 or even more interfaces)



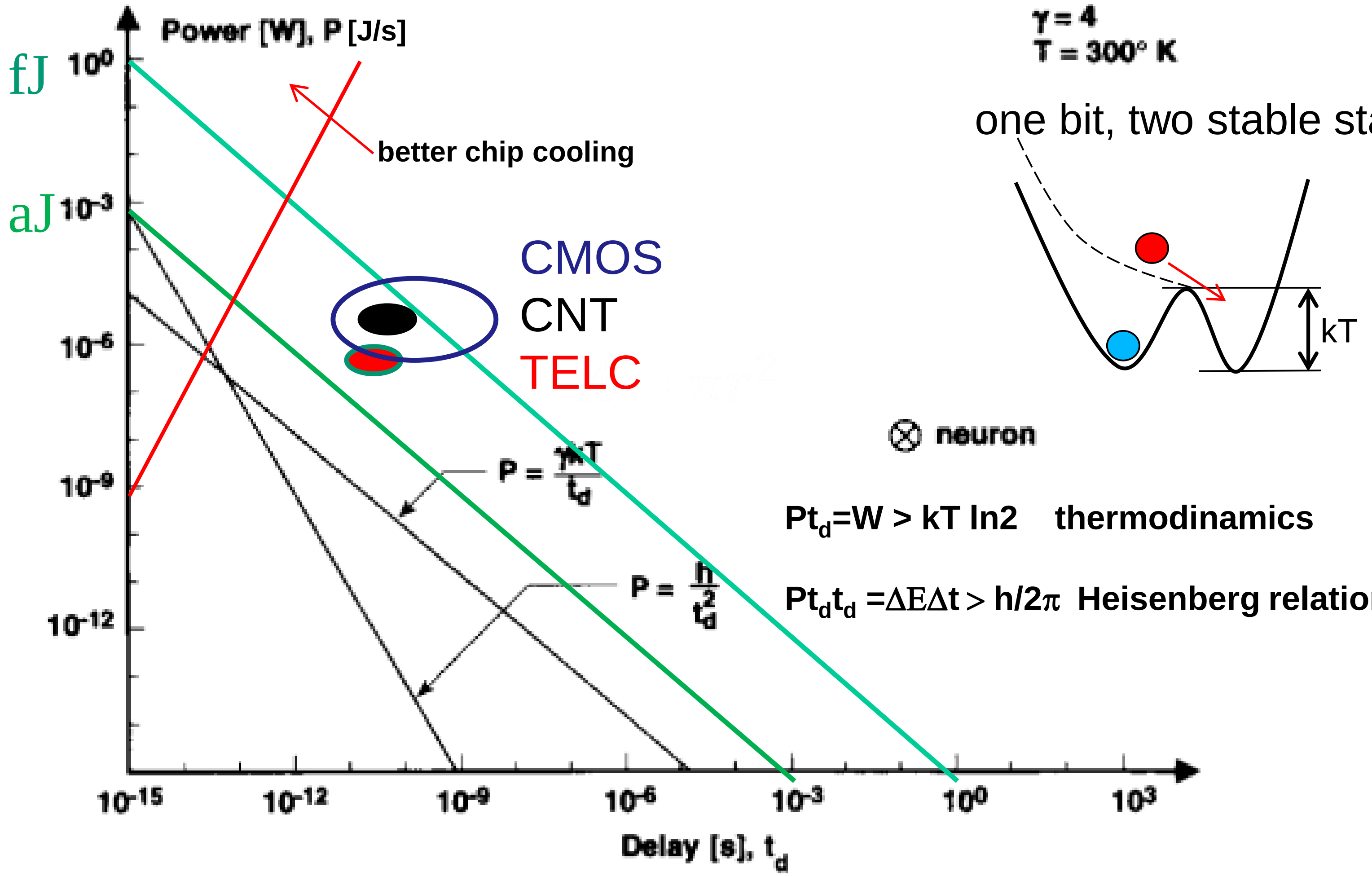
with less number of interfaces



scale down limits: depletion layers, gate-tunnel current -> direct tunnel distance: 2 nm)

scale down limits: tunnel current, size effect on MIT

$P\tau$ (power delay product), PDP: energy, related to transfer, store or process of one bit



one bit, two stable state

$Pt_d = W > kT \ln 2$ **thermodinamics**

$Pt_d t_d = \Delta E \Delta t > h/2\pi$ **Heisenberg relation**

$P\tau$ product for thermal electric gate

$$W = P\tau = L_{th}^3 \rho c_p \Delta T + L_{MIT}^3 \rho_{MIT} c_{MIT} \Delta T + L_{MIT}^3 \rho_{MIT} L$$

Energy for heating the environment + heating the MIT element itself + heat for phase transiton

where:

$L_{th} = \sqrt{\alpha t}$ thermal diffusion length (characteristic lenght at given time scale, SI units: m, value: ~10^{-8} m for 10 GHz

$\rho \quad \rho_{MIT}$ density of the environment (SiO_2) and MIT material, respectively, SI units: kg/(m^3) , value: 2650, 4600

$c_p \quad c_{MIT}$ specific heat capacity of the environment and MIT material, respectively, SI units: J/(kg K) 703 , 340-> 770

L specific latent heat, SI units: J/(kg), value: 51410

L_{MIT} characteristic size of the MIT device, value: 10^{-8} m (10 nm)

$P\tau$ product (aJ) for thermal electric gate

$$W = P\tau = L_{th}^{3}\rho c_{p}\Delta T + L_{MIT}^{3}\rho_{MIT} c_{MIT}\Delta T + L_{MIT}^{3}\rho_{MIT} L$$

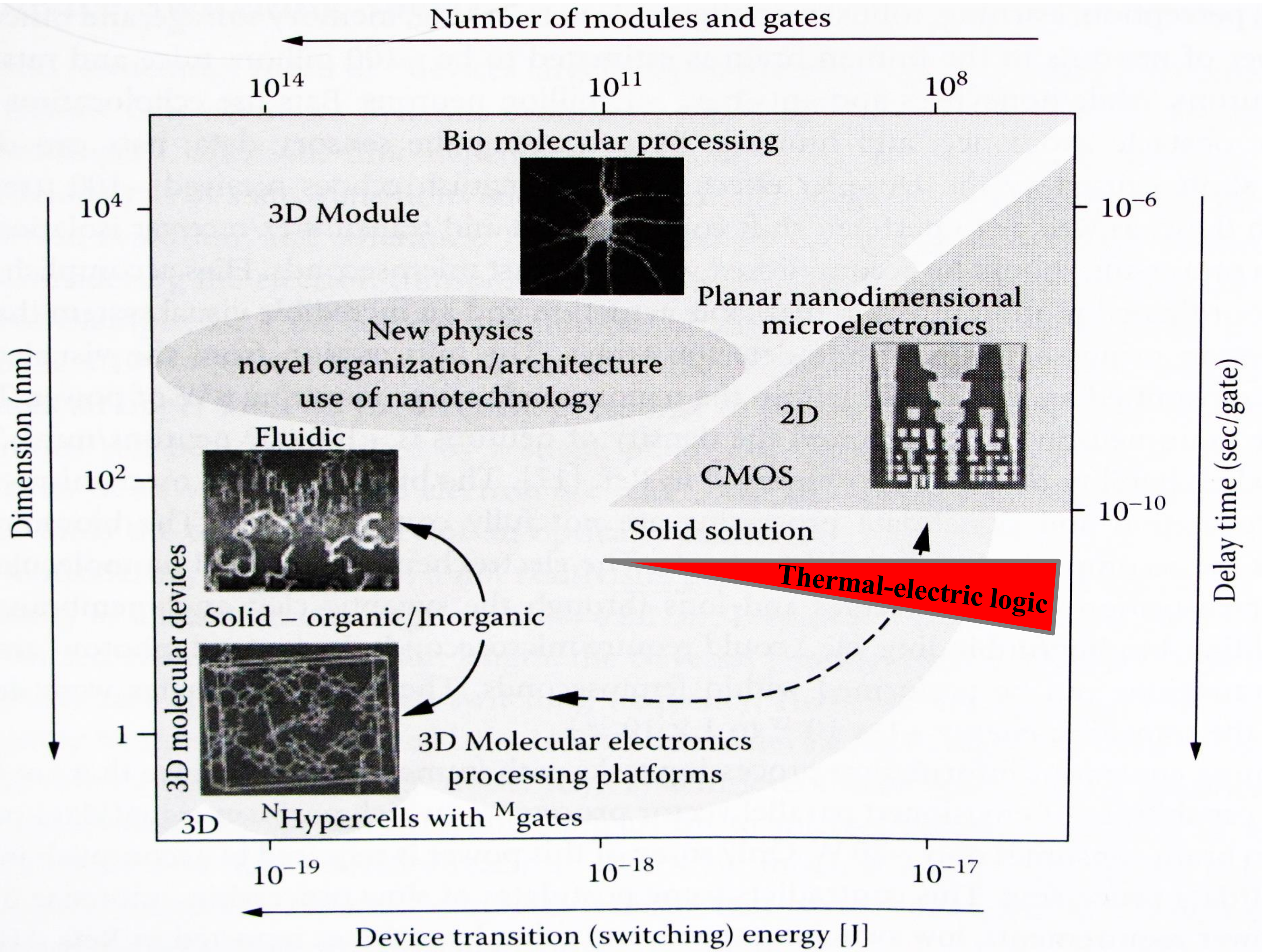
Energy for heating the environment + heating the MIT element itself + heat for phase transiton

$$W = P\tau = 19 + 16 + 236 = 271$$ aJ

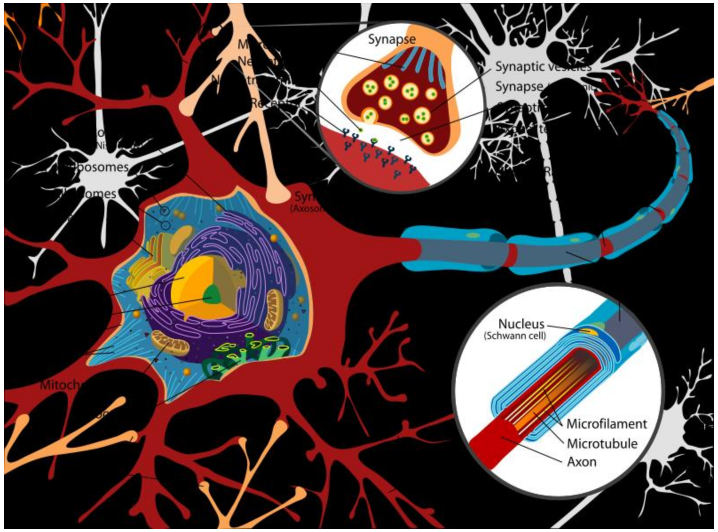
$P\tau$ product (aJ) for CNT: ~400

$P\tau$ product (aJ) for CMOS: 50-500-1000

Thermal electric logic circuit in the „gap”



The "secret" of the huge performance of the human brain (after J. von Neumann, Neumann Janos) is, that



it is analogue: higher excitation – higher response

it is digital: certain combination of excitations -> response

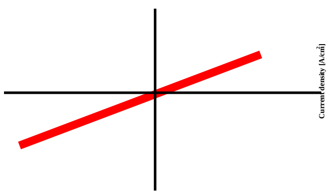
it is parallel: certain combination of excitations -> response

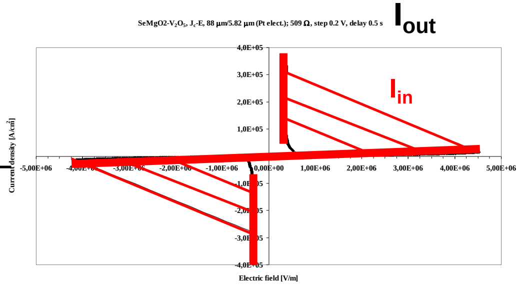
it is sequential: two (or more) subthreshold excitation within recovery time -> response (sequential AND function)

…depending on the given job!

Electro-thermal integrated circuits (systems) are:

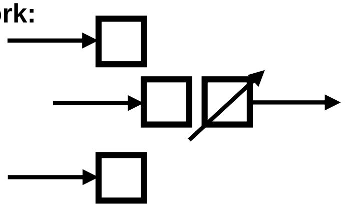
•analogue: higher excitation – higher response





•digital: certain combination of excitations -> response

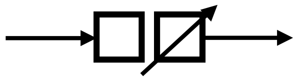
Combination network:
(AND OR) gate



•paralel: certain combination of excitations -> response

•sequential: two or (more) subthreshold excitation
within recovery time (thermal time constant) -> response (memristor)

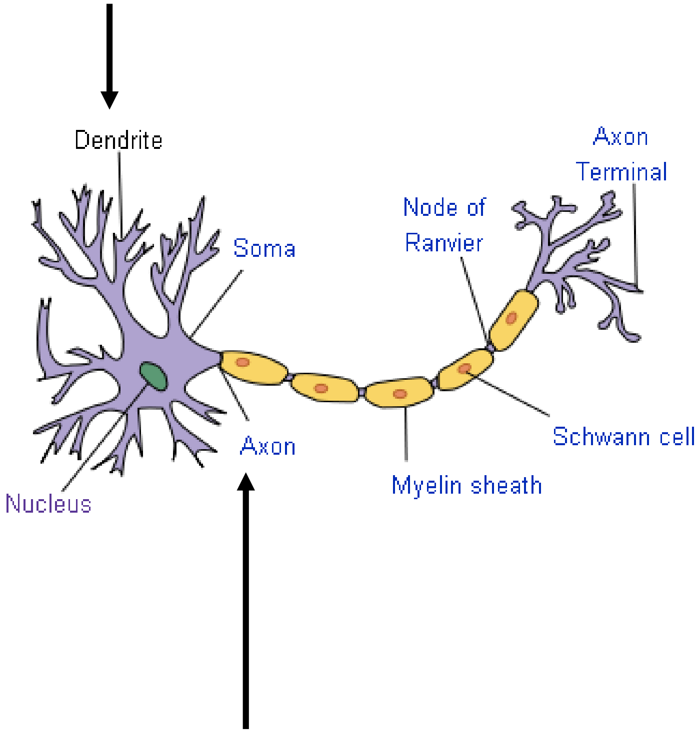
sequential: (AND) gate



…depending on the given job and timing!

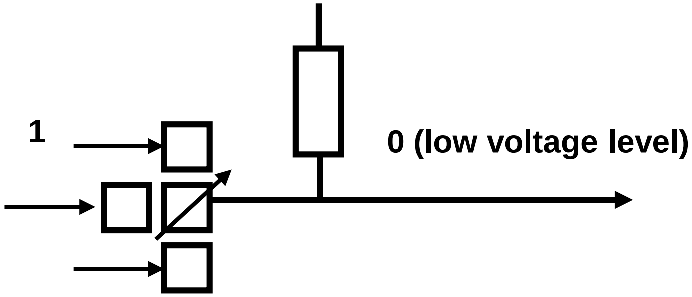
Electro-thermal integrated circuit: a bit more…

chemical coupling (diffusion of ions)

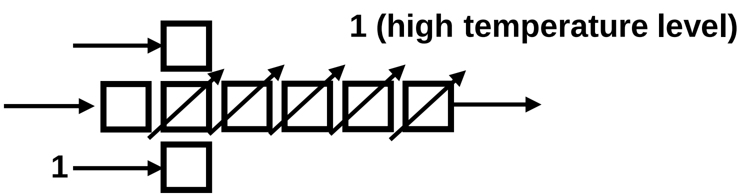


electrical coupling (for longer distances too)

- **Electrical coupling: NOR (for longer distances too)**

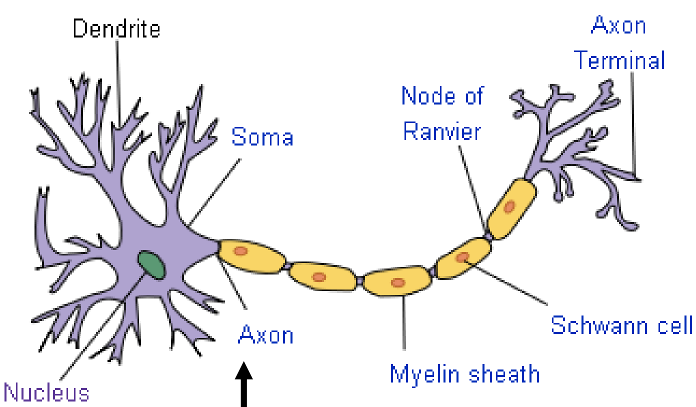


- **Thermal (diffusion) coupling: OR (for the next gate only)**



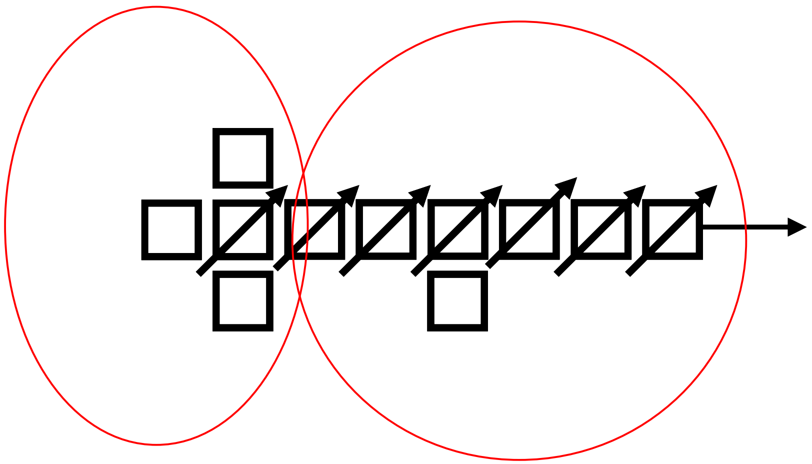
Electro-thermal integrated circuit: a bit more…

chemical coupling (diffusion of ions)



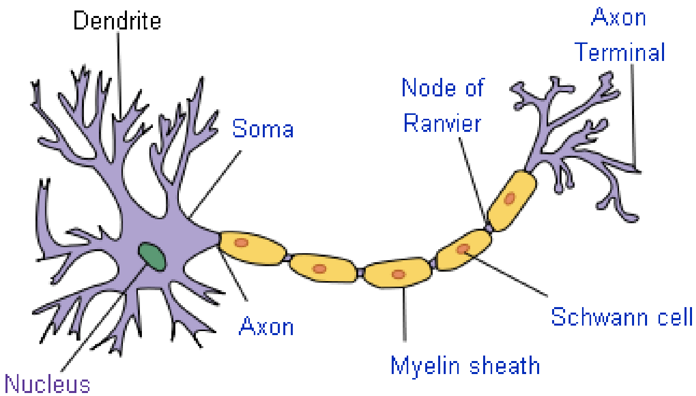
electrical coupling (for longer distances too)

gate with three inputs



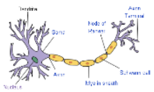
thermal transmission line even with an additional input

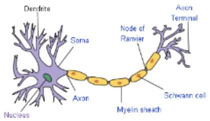
Electro-thermal integrated circuit: even more…

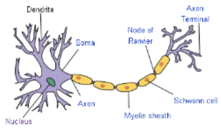


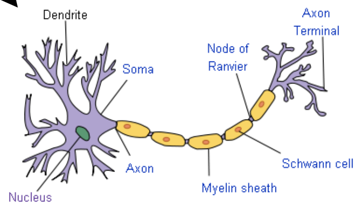
hormon release into the intercellular liquid

slow diffusion of hormons

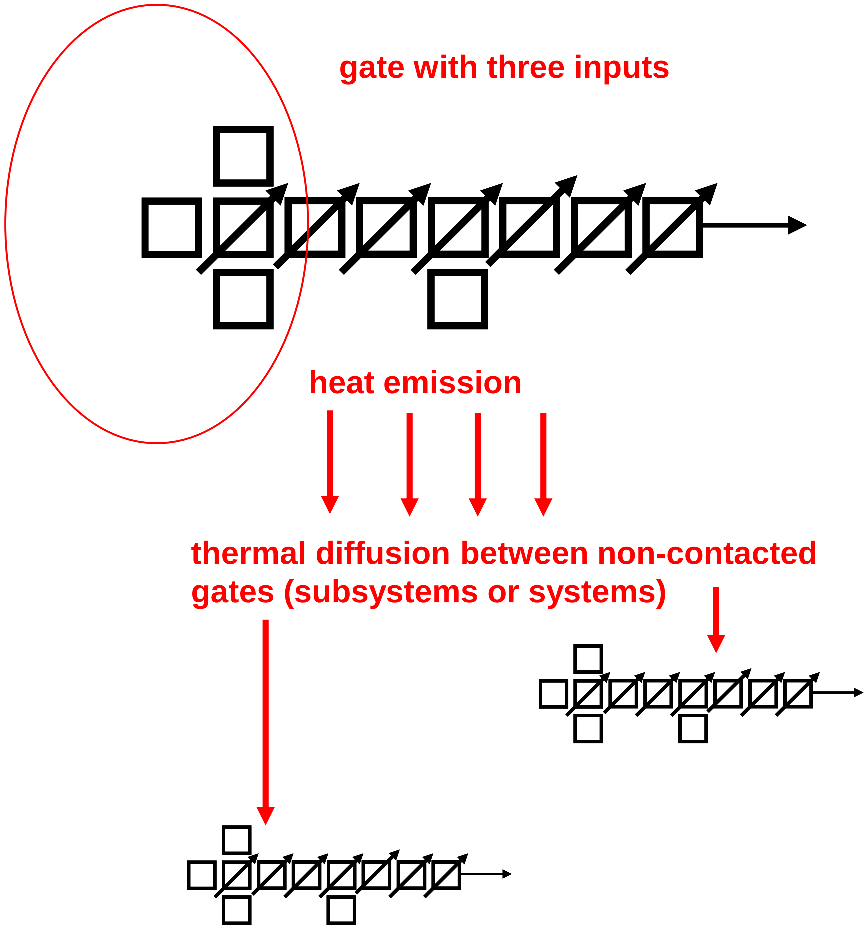






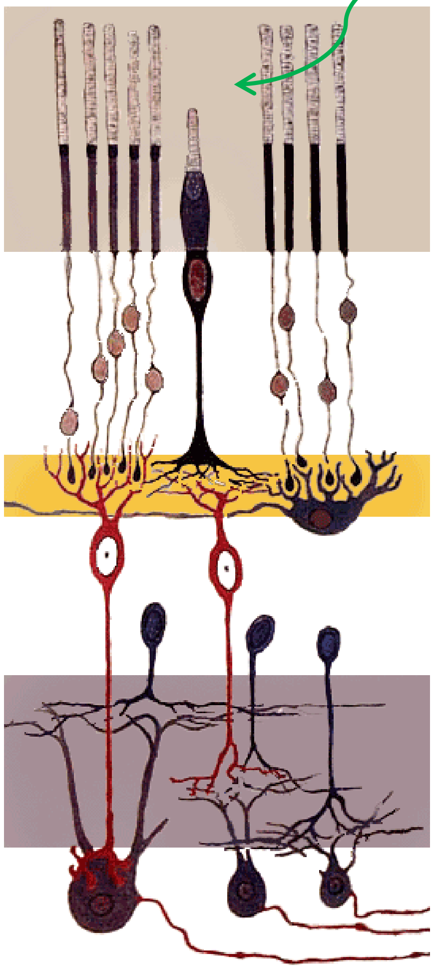


chemical coupling between non-contacted cells



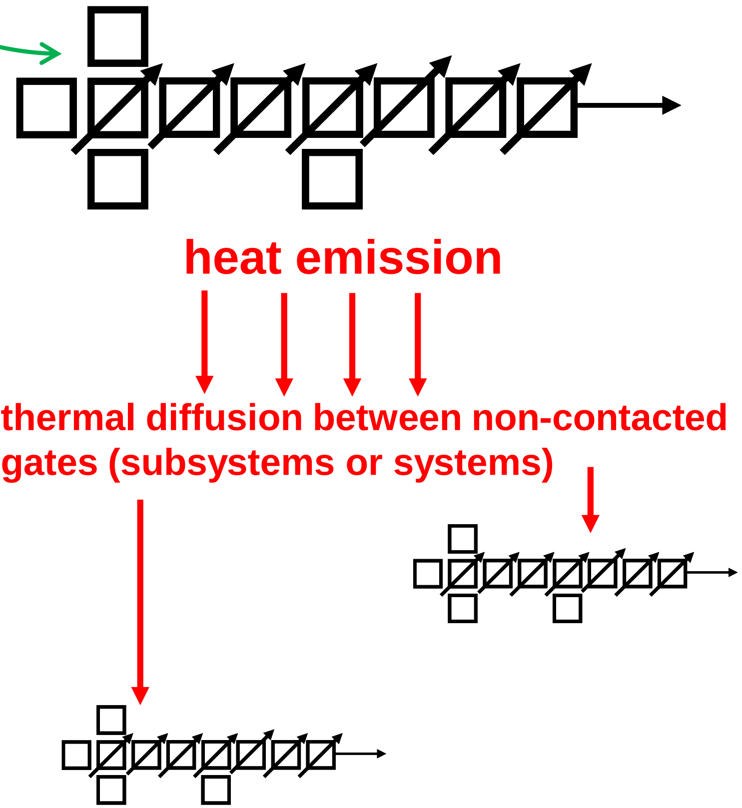
Electro-thermal integrated circuit: even more…

light excitation



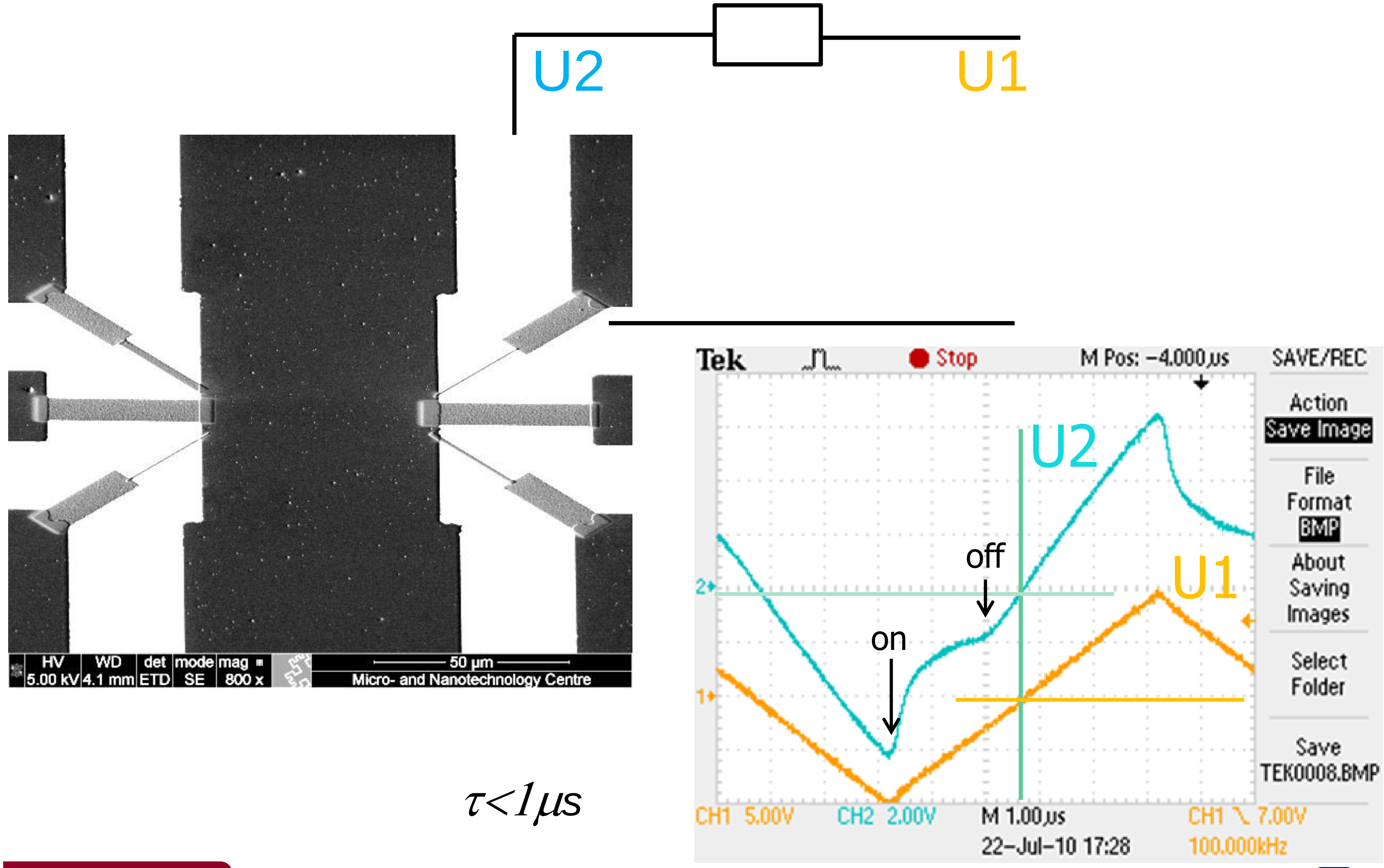
retine

gate with three inputs and light excited MIT effect



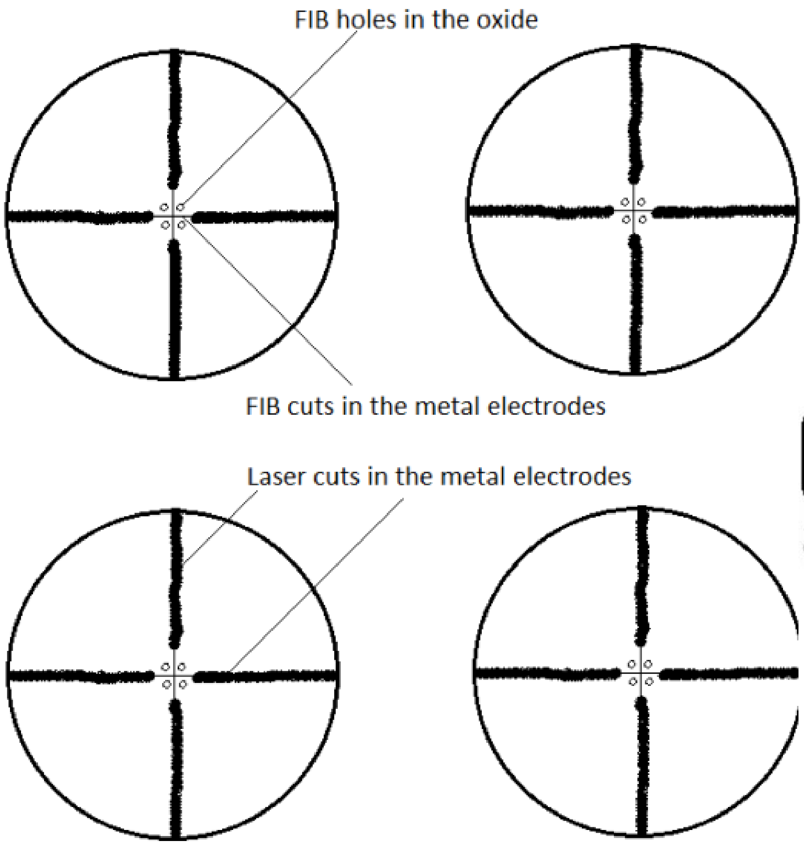
different coupling possibilities (thermal, electrical, optical): easy communication with other kind of systems

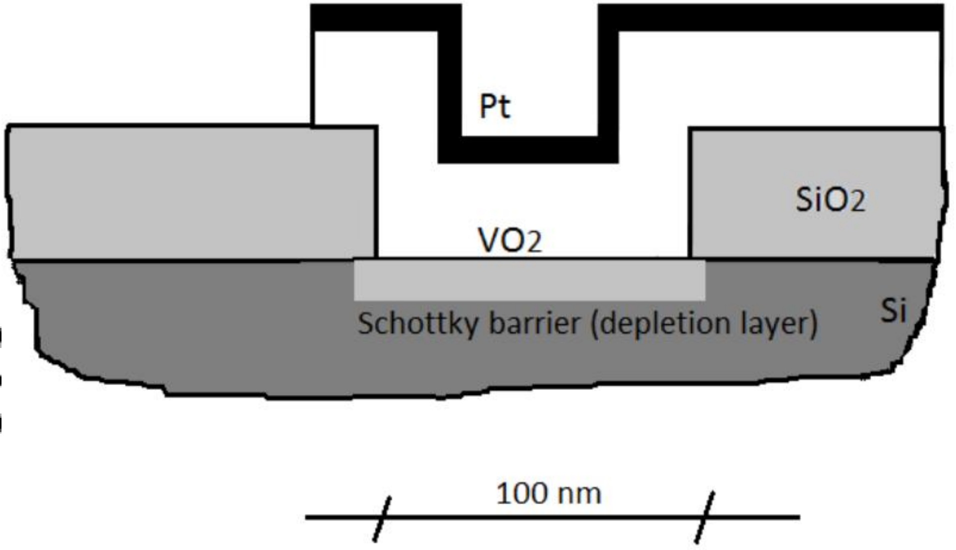
Experimental results: Nano-size VO_2 switch-on



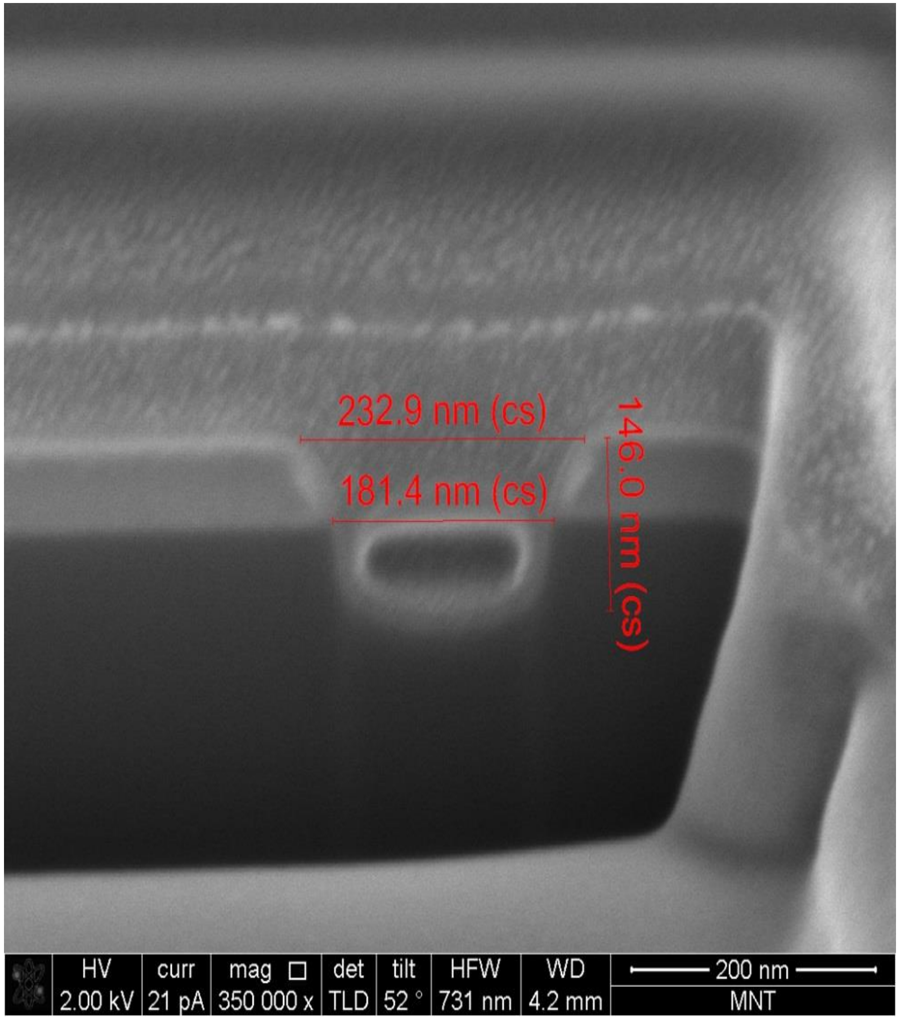
$\tau < 1\mu s$

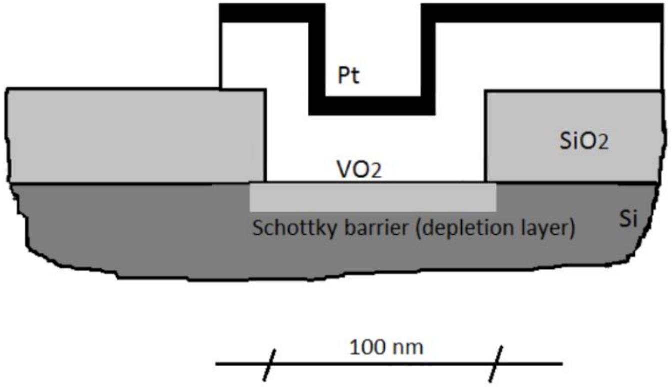
Nanosized experimental TELC gate

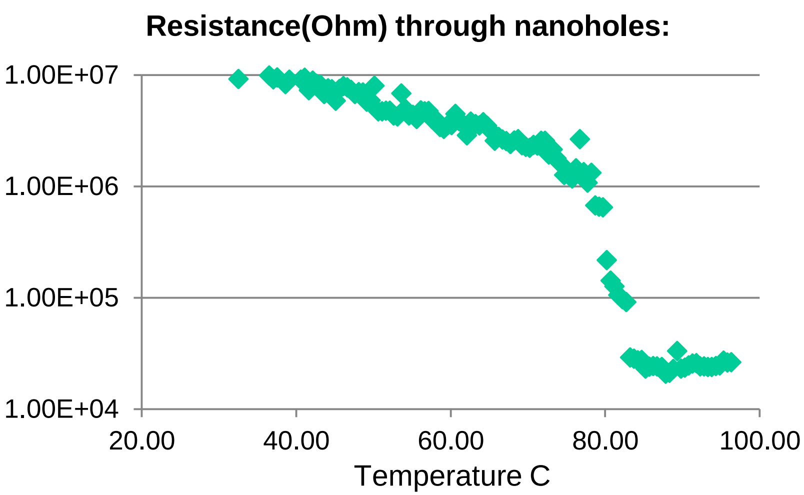


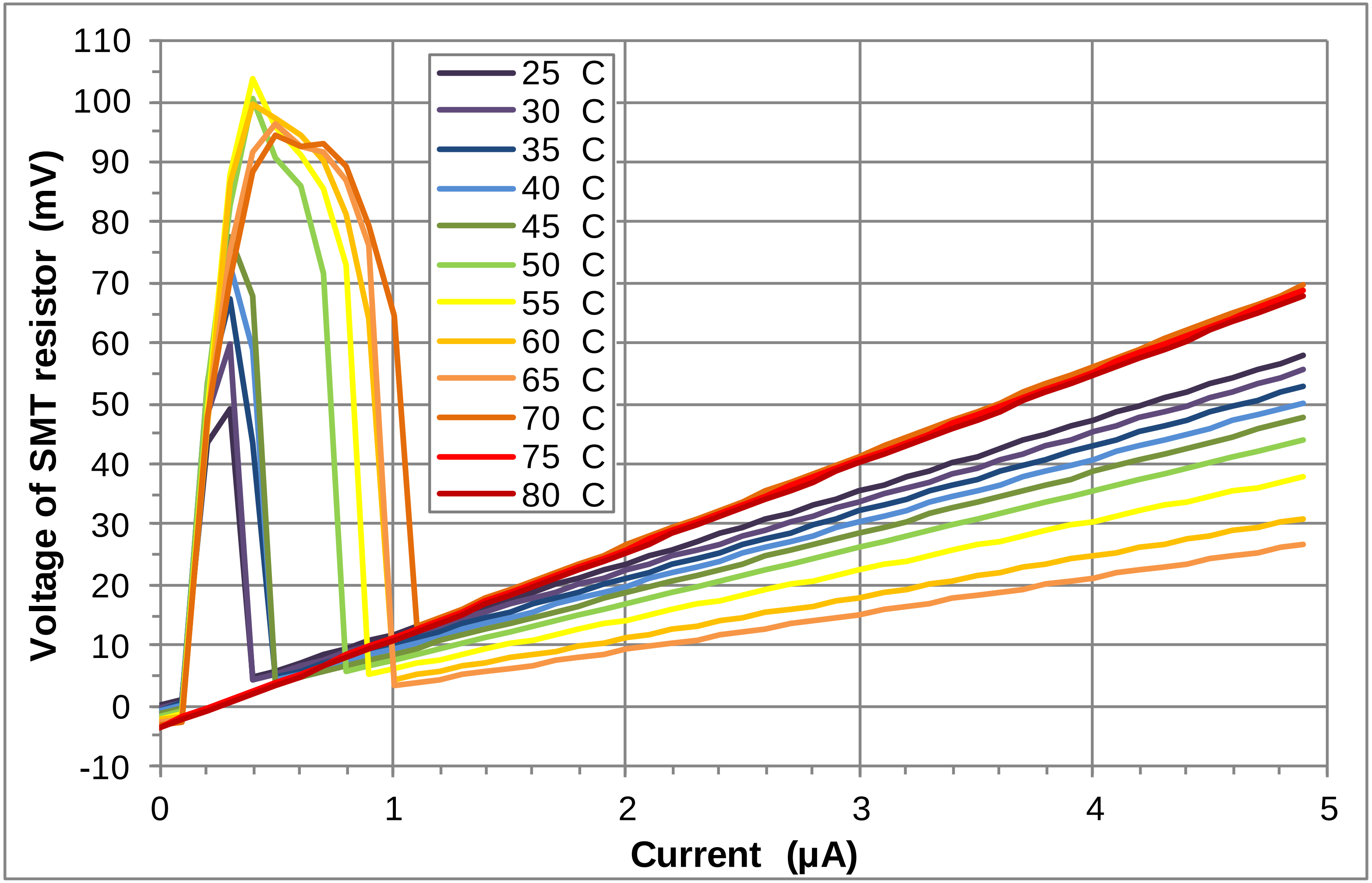


Nanosized experimental TELC gate









Switching behavior of the nm-sized, vertical SMT resistor structure, "reverse" (negative) bias with respect to the n^{++} Si substrate. It can clearly be seen that for 75 °C and above no high-resistance region is present.

SWOT

„Strength”

- extremely simple structure („bulk” resistors with common bottom electrodes, only two interfaces)
- better tolerance against radiation
- less physical limits considering the scaling down (10nm)
- compatible with the recent IC technology

„Weaknesses”

- thermal dissipation and
- cooling and temperature stabilising (thermal management)
- a very exact and very sophisticated electro-thermal-logic simulation and new design principles are needed for proper realisation

„Opportunities”

- easy communication with other part of systems (electrical or thermal coupling to CMOS, optical coupling)
- technological flexibility (horizontal, vertical or mixed realisation)
- design flexibility (signal paths for all directions-> brain like operation)

„Threats”

- there are no data about reliability of the thermal-electric computing
- the thermal transport at nm scale is still unknown field

MŰEGYETEM 1782

Budapest University of Technology and Economics

Thank You for your attention!

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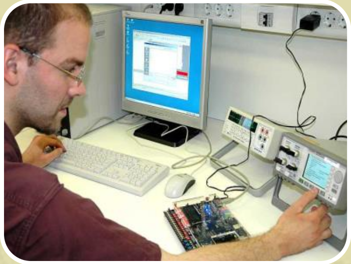
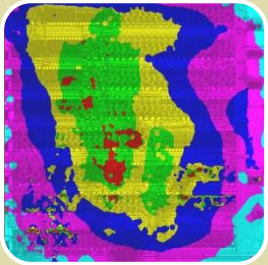
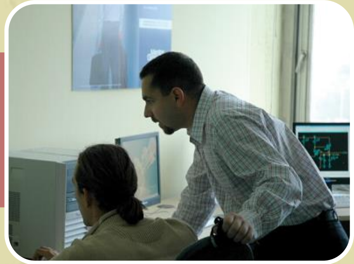
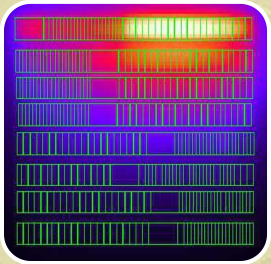
Department of Electron Devices









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